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EXAMINER	
KISS, ERIC B	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 07/26/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/777,954	MINAMIDE ET AL.	
	Examiner	Art Unit	
	Eric B. Kiss	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *27 April 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-5,7-19,23-30 and 32-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-5,7-19,23-30 and 32-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. The reply filed 27 April 2005 has been received and entered. Claims 2-5, 7-19, 23-30, and 32-37 are pending.

Information Disclosure Statement

The Cited Non-patent Document

2. The information disclosure statement filed February 7, 2001, fails to comply with the provisions of 37 CFR 1.97, 1.98 and MPEP § 609 because each publication listed in an information disclosure statement must be identified by publisher, author (if any), title, relevant pages of the publication, date, and place of publication (see 37 CFR 1.98(b)(5). It has been placed in the application file, but the information referred to therein has not been considered as to the merits. Applicant is advised that the date of any re-submission of any item of information contained in this information disclosure statement or the submission of any missing element(s) will be the date of submission for purposes of determining compliance with the requirements based on the time of filing the statement, including all certification requirements for statements under 37 CFR 1.97(e). See MPEP § 609 ¶ C(1).

Because the cited "LadderWORK" document appears to be a printout from a web page, Applicant is reasonably expected to be able to produce the name of the publisher (presumably MicroSHADOW Research), place of publication (*e.g.*, the URL for the web page, which Applicant admits having knowledge of; see p. 13 of Applicant's remarks), date (*e.g.*, the date the web page was accessed/printed, and, preferably, the date the document was published, which might appear, for example, at the end of the document, on a page not submitted—four pages

were received), and relevant pages (*e.g.*, the number of pages), as part of a complete citation of the provided document. Failing this, Applicant's information disclosure statement does not comply with the provisions of 37 CFR 1.98.

The Cited Foreign Patent Document

3. Each information disclosure statement must include a concise explanation of the relevance, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information listed that is not in the English language. The concise explanation may be either separate from the specification or incorporated therein with the page(s) and lines of the specification where it is incorporated being noted in the IDS. Where the information listed is not in the English language, but was cited in a search report or other action by a foreign patent office in a counterpart foreign application, the requirement for a concise explanation of relevance can be satisfied by submitting an English-language version of the search report or action which indicates the degree of relevance found by the foreign office. See MPEP §609.

It is noted that Applicant has provided an English-language abstract for the foreign reference. Submission of an English language abstract of a reference may fulfill the requirement for a concise explanation. See MPEP §609. "The duty of candor does not require that the Applicant translate every foreign reference, but only that the Applicant refrain from submitting partial translations and concise explanations that it knows will misdirect the Examiner's attention from the reference's relevant teaching." See Semiconductor Energy Laboratory Co. v. Samsung Electronics Co., 204 F.3d 1368, 54 USPQ2d 1001 (Fed. Cir. 2000). Accordingly, the Applicant-

provided English-language abstract has been considered (as was indicated by the Examiner's initials on the form PTO-1449 attached to the Office action mailed 21 May 2004), and is assumed to reflect the most relevant teachings contained within the reference that is not in the English language, as it is presently understood by the individual designated in 37 CFR 1.56(c) most knowledgeable about the content of the information listed.

Response to Amendment

4. The substitute declaration has been received and is acceptable. The objection to the declaration is withdrawn.

5. The amendments to the specification and abstract appropriately address the corresponding objections, which are accordingly withdrawn.

6. The amendment to claim 9 appropriately addresses the objection to claim 9, based on an informality. Accordingly, this objection is withdrawn.

7. Applicant's comments with regard to the objection to claim 17 have been fully considered. The objection to claim 17 is withdrawn.

8. Applicant's amendments to the claims do not appropriately address the rejection under 35 U.S.C. §112, first paragraph. Accordingly, this rejection is maintained and reproduced below.

9. Applicant's amendments to the claims appropriately address the rejection under 35 U.S.C. §112, second paragraph. Accordingly, this rejection is withdrawn.

Response to Arguments

10. Applicant's arguments filed 27 April 2005 have been fully considered but they are not persuasive.

a. In response to Applicant's arguments on p. 15, in paragraph 4, Applicant's allegation that the rejection is not articulated, citing 37 CFR 1.104(c)(2), is without merit and is wholly unpersuasive. As Applicant notes, for each claim limitation, the rejection cites a section of the applied reference (thus meeting the requirement of 37 CFR 1.104(c)(2)).

b. In response to Applicant's arguments on p. 15, in paragraph 5, [Kim99] discloses an implementation using the TMS320C40 digital signal processor (section 3.2). This processor has both pipeline logic and a cache contributing to its performance. The Examiner suggests that Applicant consider the specification sheet for said processor as provided with the Office action mailed 21 May 2004. Further, the excerpts from "TMS320C4x User's Guide," cited with this action, very clearly describe each of these inherent features (see the description of the cache in chapter 4 and the description of the pipeline logic in chapter 8).

c. In response to Applicant's arguments on p. 15, in the last paragraph, continuing onto p. 16, the Examiner respectfully submits that the readily apparent reason that the previous Office

action does not articulate how Kim teaches converting blocks into high-level-language control programs is that this is a newly claimed feature. These arguments are moot in view of the new grounds of rejection set forth below.

d. In response to Applicant's arguments on p. 16, in paragraph 4, the Examiner maintains that the use of underlying apparatus components is inherent in determining the execution times of the modified programs as disclosed. Put very simply, one cannot measure an execution time of a program without executing the program, and one cannot execute the program without such an apparatus containing the necessary hardware to carry out such execution. Further, [Kim99] appears to disclose the use of a TMS320C40 digital signal processor to carry out such execution.

e. In response to Applicant's arguments on p. 16, in the last paragraph, continuing onto p. 17, [Kim99] shows a predetermined rung in a ladder diagram (for example, Fig. 4(a)) and a corresponding plurality of blocks (for example, Fig. 4(c) and Fig. 5).

f. In response to Applicant's arguments on p. 17, in paragraph 2, [Kim99] discloses a plurality of blocks at a predetermined rung (for example, the blocks illustrated in Fig. 4(c) and Fig. 5, corresponding to the predetermined rung illustrated in Fig. 4(a)). [Kim99] further discloses storing labels corresponding to these blocks in a symbol table for use in branching (jumping) by the digital signal processor (see, for example, the last paragraph of column 1 on p. 3, continuing onto the second column of p. 3).

g. In response to Applicant's arguments on p. 17, in paragraph 3, the Examiner respectfully submits that the PLC disclosed in [Kim99] is a common input/output device.

Claim Objections

11. Claims 23 and 32 are objected to because of the following informalities:

"directly-executable" in line 13 of claim 23 should presumably read --directly executable--.

"pattern-matching-table" in line 12 of claim 32 should presumably read --pattern-matching table--.

"directly-executable" in line 13 of claim 32 should presumably read --directly executable--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

12. The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

13. Claims 12-19, 27, 28, 36, and 37 are rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the enablement requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to enable one skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Regarding claims 12, 19, 27, and 27, the phrase "universal computer" is not sufficiently defined in the specification or in the prior art to the extent necessary for one of ordinary skill in the art to make and use the described invention within any reasonable level of experimentation. In the interest of compact prosecution, the Examiner subsequently ignores all occurrences of the word "universal" in the claims for the purpose of further examination.

Claims 13-18, 36, and 27 are rejected based on limitations recited in their respective parent claims and rejected as set forth above.

Claim Rejections - 35 USC § 102

14. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

15. Claims 1, 2, 4-9, 11-16, 18, 21, 22, 25-27, and 31 are rejected under 35 U.S.C. 102(b) as being anticipated by Hyung Seok Kim, et al., "A Translation Method of Ladder Diagram on PLC with Application to a Manufacturing Process," 1999 (hereinafter [Kim99]).

As per claim 2, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-development supporting apparatus comprising a compiler which compiles the control program into codes directly executable by a microprocessor that includes an acceleration unit (see, for example, section 3 on pp. 2-4).

As per claim 5, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-development supporting apparatus comprising: a control-program dividing unit which divides the control program into a plurality of blocks (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of the blocks into execution codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4). [Kim99] further discloses the programmable controller including a microprocessor having an acceleration unit (see, for example, section 3.2 on p. 4).

As per claim 7, [Kim99] further discloses the control program being a ladder logic diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit dividing the control program into a plurality of blocks at a predetermined rung in the ladder diagram to generate a program file for every block concerned (see, for example, section 3 on pp. 2-4).

As per claim 8, [Kim99] further discloses the control program being a ladder diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit dividing the control program into a plurality of blocks at a predetermined rung serving as a jump destination for a jump instruction in the ladder diagram to generate a program file for every block (see, for example, section 3 on pp. 2-4).

As per claim 9, [Kim99] further discloses the control-program being a ladder diagram or an instruction list generated from the ladder diagram, and the control-program dividing unit extracting at least some rungs including instruction to a common input or output device from the

ladder diagram, at least some of the rungs extracted constituting one block, and generating a program file for every block (see, for example, section 3 on pp. 2-4).

As per claim 25, [Kim99] discloses a storing unit which stores the execution codes; a microprocessor including an acceleration unit, and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language, the control-program-development supporting apparatus having a compiler which compiles the control program into codes directly executable by a microprocessor that includes an acceleration unit (see, for example, section 3 on pp. 2-4).

As per claim 26, [Kim99] discloses a storing unit which stores the execution codes; a microprocessor which includes an acceleration unit and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language, the control-program-development supporting apparatus having, a control-program dividing unit which divides the control program into a plurality of blocks (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of the blocks into execution codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4).

As per claims 33 and 35, [Kim99] discloses the acceleration unit including pipeline logic and a cache (inherent features of the TMS320C40 digital signal processor).

16. Claims 23, 24, 29, 32, and 34 are rejected under 35 U.S.C. 102(b) as being anticipated by "TMS320C4x User's Guide," May 1999, Texas Instruments (hereinafter [TI99]).

As per claim 23, [TI99] discloses a storing unit which stores the control program (see, for example, p. 4-1, paragraph 3); an instruction counting unit which counts the appearance frequency of each instruction used for execution of the control program (see, for example, section 4.3.1 on pp. 4-10 through 4-12); a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit (see, for example, section 4.3.1 on pp. 4-10 through 4-12); and an interpreting unit which executes the control program while pattern-matching the instructions listed in the pattern-matching-table in order and interpreting the control program into codes directly executable by the programmable controller (see, for example, the description of the Instruction Cache in section 4.3 on pp. 4-10 through 4-14).

As per claim 24, [TI99] discloses an instruction counting unit which counts the appearance frequency of each instruction used for execution of the control program (see, for example, section 4.3.1 on pp. 4-10 through 4-12); a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit (see, for example, section 4.3.1 on pp. 4-10 through 4-12); and a compiler which compiles the control program into codes directly executable by the programmable controller while pattern-matching the instructions listed in the pattern matching table in order (see, for example, p. vii, the discussion of "TMS320 Floating-Point DSP Optimizing C Compiler User's Guide").

As per claim 29, [TI99] discloses a storing unit which stores the control program (see, for example, p. 4-1, paragraph 3); a microprocessor including an acceleration unit and directly executing the execution codes (see, for example, the discussion of the CPU on pp. 2-4 through 2-10, along with the discussion of the instruction cache in section 4.3 on pp. 4-10 through 4-14); a control-program-development supporting apparatus that develops a control program described with a sequential-control language, and having, an instruction counting unit which counts the appearance frequency of each instruction used for execution of the control program (see, for example, section 4.3.1 on pp. 4-10 through 4-12); a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit (see, for example, section 4.3.1 on pp. 4-10 through 4-12); and a compiler which compiles the control program into codes directly executable by the programmable controller while pattern-matching the instructions listed in the pattern matching table in order (see, for example, p. vii, the discussion of "TMS320 Floating-Point DSP Optimizing C Compiler User's Guide").

As per claim 32, [TI99] discloses a storing unit which stores the control program (see, for example, p. 4-1, paragraph 3); an instruction counting unit which counts the appearance frequency of each instruction used for execution of the control program (see, for example, section 4.3.1 on pp. 4-10 through 4-12); a pattern-matching-table generating unit which generates a pattern-matching table in which instructions are listed starting with the highest appearance frequency in accordance with results counted by the instruction-counting unit (see, for example, section 4.3.1 on pp. 4-10 through 4-12); and an interpreting unit which executes the control program while pattern-matching the instructions listed in the pattern-matching-table in

order and interpreting the control program into codes directly executable by the programmable controller (see, for example, the description of the Instruction Cache in section 4.3 on pp. 4-10 through 4-14); and a compiler which compiles the control program into codes directly executable by the programmable controller while pattern-matching the instructions listed in the pattern matching table in order (see, for example, p. vii, the discussion of "TMS320 Floating-Point DSP Optimizing C Compiler User's Guide").

As per claim 34, [TI99] discloses the use of pipeline logic and a cache (see the description of the cache in chapter 4 and the description of the pipeline logic in chapter 8).

Claim Rejections - 35 USC § 103

17. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

18. Claims 4 and 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of *Mastering Excel 97*, 4th ed., 1997, by Thomas Chester and Richard H. Alden (hereinafter [ChA97]).

As per claims 4 and 11, in addition to the disclosure applied to claims 2 and 5, [Kim99] further discloses a processing-time rough-estimating unit which relates a sample program having a known processing time with the control program corresponding to the execution codes to

estimate sequential-processing execution time of a programmable controller (see, for example, section 4 on pp. 4-5; the use of underlying apparatus components is inherent in determining the execution times of the modified programs as disclosed; [Kim99] further appears to disclose the use of the TMS320C40 digital signal processor for such a purpose, as disclosed, for example, in section 3.2 on p. 4). [Kim99] fails to expressly disclose the use of a relating table in implementing such relating. However, the calculated execution time equation (equation (2) on p. 5) contains indexed values (*e.g.*, T_i, where i is an index from 1 to 6) related to the execution times of various ladder diagram mnemonics (see Figure 7). As is well known in the computer programming art, a table is an indexed data structure, allowing data to be retrieved and processed based on a unique index. An example of the use of a table (for example, a spreadsheet) in performing a calculation can be found in [ChA97] (see, for example, the loan calculator described on pp. 114-117). It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to include the use of such a table in the execution time calculation of [Kim99] as tables are well suited to such tasks involving calculations performed on indexed data.

19. Claims 12-16, 27, and 36 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of U.S. Patent No. 5,504,902 to McGrath et al.

As per claim 12, [Kim99] discloses a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-program-development supporting apparatus comprising: a control-program dividing unit which divides the control program into a plurality of blocks (see, for example, section 3 on

pp. 2-4); a control-program converting unit which converts at least some of the blocks into advanced-language control programs described with a computer-readable advanced language for every block (see, for example, section 3 on pp. 2-4); and a compiler which compiles at least some of the computer-readable advanced programming languages corresponding to every block into codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose the "advanced language" being a high-level language. However, McGrath et al. teaches such a conversion from a ladder-based language to a high-level language (see, for example, col. 4, line 59, through col. 5, line 17). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the conversion of [Kim99] to including such a high-level language. One would be motivated to do so to provide an additional means to edit and debug a control program.

As per claims 13-16, see the disclosure applied above to claims 5 and 7-9. For reasons stated above, such claims also would have been obvious.

As per claim 27, [Kim99] discloses a storing unit which stores the execution codes (see, for example, section 3 on pp. 2-4); a microprocessor which includes an acceleration unit and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program, described with a sequential-control language, the control-program-development supporting apparatus having, a control-program dividing unit which divides the control-program into a plurality of blocks (see, for example, section 3 on pp. 2-4); a control-program converting unit which converts at least some of the blocks into advanced-language control programs described with a universal-computer-readable advanced language for every block (see, for example, section 3 on pp. 2-4);

and a compiler which compiles at least some of universal-computer-readable advanced programming languages corresponding to every block into codes directly executable by a programmable controller (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose the "advanced language" being a high-level language. However, McGrath et al. teaches such a conversion from a ladder-based language to a high-level language (see, for example, col. 4, line 59, through col. 5, line 17). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the conversion of [Kim99] to including such a high-level language. One would be motivated to do so to provide an additional means to edit and debug a control program.

As per claim 36, [Kim99] discloses the acceleration unit including pipeline logic and a cache (inherent features of the TMS320C40 digital signal processor). Therefore, for reasons stated above, such a claim also would have been obvious.

20. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of *McGrath et al.*, as applied to claim 12 above, and further in view of [ChA97].

As per claim 18, in addition to the disclosure applied to claim 12, [Kim99] further discloses a processing-time rough-estimating unit which relates a sample program having a known processing time with the control program corresponding to the execution codes to estimate sequential-processing execution time of a programmable controller (see, for example, section 4 on pp. 4-5; the use of underlying apparatus components is inherent in determining the execution times of the modified programs as disclosed; [Kim99] further appears to disclose the

use of the TMS320C40 digital signal processor for such a purpose, as disclosed, for example, in section 3.2 on p. 4). [Kim99] fails to expressly disclose the use of a relating table in implementing such relating. However, the calculated execution time equation (equation (2) on p. 5) contains indexed values (*e.g.*, T_i, where i is an index from 1 to 6) related to the execution times of various ladder diagram mnemonics (see Figure 7). As is well known in the computer programming art, a table is an indexed data structure, allowing data to be retrieved and processed based on a unique index. An example of the use of a table (for example, a spreadsheet) in performing a calculation can be found in [ChA97] (see, for example, the loan calculator described on pp. 114-117). It would have been obvious to one of ordinary skill in the computer art at the time the invention was made to include the use of such a table in the execution time calculation of [Kim99] as tables are well suited to such tasks involving calculations performed on indexed data.

21. Claims 3 and 10 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99], as applied to claims 2, 5, and 12 above, in view of Alfred V. Aho, et al., "Compilers: Principles, Techniques, and Tools," 1988 (hereinafter [Aho88]).

As per claims 3 and 10, in addition to the disclosure applied above to claims 2 and 5, [Kim99] discloses an optimization filtering unit which reconstructs the control program into an optimum code system by rearranging codes for locally arranging instructions for a common input or output device, wherein a control program optimized by said optimization filtering unit is newly used as the control program (see, for example, section 3 on pp. 2-4). [Kim99] fails to

expressly disclose excluding not-cited variables and redundant codes. However, [Aho88] teaches such well-known compiler optimization techniques as dead/redundant/unreachable code elimination (see, for example, section 9.9 on pp. 554-557; and section 10.2 on pp. 592-598). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the optimizing compiler framework disclosed by [Kim99] to include such known optimization techniques as taught by [Aho88]. One would be motivated to do so to improve the quality of resulting generated code.

22. Claim 17 is rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] and *McGrath et al.*, as applied to claim 12 above, in view of [Aho88].

As per claim 17, in addition to the disclosure and teachings applied above to claim 12, [Kim99] discloses an optimization filtering unit which reconstructs the control program into an optimum code system by rearranging codes for locally arranging instructions for a common input or output device, wherein a control program optimized by said optimization filtering unit is newly used as the control program (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose excluding not-cited variables and redundant codes. However, [Aho88] teaches such well-known compiler optimization techniques as dead/redundant/unreachable code elimination (see, for example, section 9.9 on pp. 554-557; and section 10.2 on pp. 592-598). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the optimizing compiler framework disclosed by [Kim99] to include such known optimization techniques as taught by [Aho88]. One would be motivated to do so to improve the quality of resulting generated code.

23. Claims 19, 28, and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of *McGrath et al.* and Jonathan B. Rosenberg, "How Debuggers Work: Algorithms, Data Structures, and Architecture," 1996 (hereinafter [Ros96]).

As per claims 19 and 28, [Kim99] discloses a storing unit which stores execution codes (see, for example, section 3 on pp. 2-4); a microprocessor including an acceleration unit (see, for example, section 3.2 on p. 4) and directly executing the execution codes (see, for example, section 3 on pp. 2-4); and a control-program-development supporting apparatus that develops a control program described with a sequential-control language (see, for example, section 3 on pp. 2-4), having a control-program converting unit which converts a control program into an advanced-programming-language control program described with a computer-readable advanced programming language (see, for example, section 3 on pp. 2-4).

[Kim99] fails to expressly disclose the "advanced language" being a high-level language. However, McGrath et al. teaches such a conversion from a ladder-based language to a high-level language (see, for example, col. 4, line 59, through col. 5, line 17). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the conversion of [Kim99] to including such a high-level language. One would be motivated to do so to provide an additional means to edit and debug a control program.

[Kim99] fails to expressly disclose a debugging-code generating unit which generates a debugging control program by inserting a line number into a part corresponding to each line, constituting the instruction list in source codes, constituting the advanced-programming-

language control program; and a debugging executing unit which displays each line of the instruction list and the execution part of the advanced-programming-language control program by relating the former with the latter. However, [Ros96] teaches that debuggers are critical tools for software development (see, for example, p. 1, line 1). [Ros96] further teaches that showing source code line correspondence is part of the most important information the programmer needs during debugging, namely program context information (see, for example, "Context Is the Torch in a Dark Cave" on pp. 9-11) and that the developer of an application who is using a debugger has a lot to gain if the original source code is mapped directly to the application's machine code (see, for example, "Source-level (Symbolic) versus Machine-level" on p 12). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the system of [Kim99] to include such program code line number correspondence as per the teachings of [Ros96]. One would be motivated to do so to allow for efficient debugging of code under development.

As per claim 37, [Kim99] discloses the acceleration unit including pipeline logic and a cache (inherent features of the TMS320C40 digital signal processor). Therefore, for reasons stated above, such a claim also would have been obvious.

24. Claim 30 is rejected under 35 U.S.C. 103(a) as being unpatentable over [Kim99] in view of Brenda S. Baker, et al., "Compressing Differences of Executable Code," 1999 (hereinafter [Bak99]).

As per claim 30, [Kim99] discloses a programmable controller comprising a control-program-development supporting apparatus that develops a control program described with a sequential-control language, said control-program-development supporting apparatus comprising a compiler which compiles the control program into codes directly executable by a microprocessor that includes an acceleration unit (see, for example, section 3 on pp. 2-4); a first storing unit which stores the execution codes and a second storing unit for storing newly created execution code and a microprocessor for direct execution of the execution codes (see, for example, section 3 on pp. 2-4). [Kim99] fails to expressly disclose the second storing unit storing data for the difference between an execution code stored in the first storing unit and a new execution code and a patch processing unit which changes an execution code currently executed into a new execution code at a predetermined timing in accordance with the difference data and continuously executing the changed execution code. However, [Bak99] teaches the use of patches that encode the differences between two versions of a program as one of the most common ways to deliver such changes (see, for example, the Abstract). [Bak99] further discloses the necessary mechanism by which such patches can be generated and applied (see, for example, section 2 on pp. 3-4 and section 3 on p. 4). Therefore, it would have been obvious to one of ordinary skill in the computer art at the time the invention was made to modify the system of [Kim99] to include such patching based on differences between an existing program and an updated program as per the teachings of [Bak99]. One would be motivated to do so to provide updates in an efficient manner by transmitting smaller files.

Conclusion

25. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

The following cited documents contain descriptions of converting from sequential logic to high-level programming language code:

US 5,285,376 (STRUGER et al.) see, for example, col. 9, line 23, through col. 10, line 68;

US 5,498,954 (BASSETT et al.) see, for example, col. 4, lines 37-47;

US 5,508,909 (MAXWELL et al.) see, for example, col. 6, line 52, through col. 7, line 14;

US 5,857,093 (BRADFORD) see, for example, col. 4, lines 9-18.

The following cited document contains a description of an execution time estimation using stored known timing information:

US 5,857,093 (BRADFORD) see the entire document.

26. Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Eric B. Kiss whose telephone number is (571) 272-3699. The Examiner can normally be reached on Tue. - Fri., 7:00 am - 4:30 pm. The Examiner can also be reached on alternate Mondays.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Tuan Dam, can be reached on (571) 272-3695. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Any inquiry of a general nature should be directed to the TC 2100 Group receptionist: 571-272-2100.

EBK /EBK
July 19, 2005

WEI Y. ZHEN
PRIMARY EXAMINER